

Introduction

This document describes the operation and use of a test bitstream for the FCRAM interface on the LatticeEC™ Advanced evaluation board or the LatticeXP™ Advanced evaluation board. This design implements an FCRAM memory controller to test the on-board FCRAM memory. The maximum operating frequency of this design is 133.33MHz for both LFEC20E-5F672C and LFXP10C-5F388C devices on the two boards respectively.

Note: All references in this document to the LatticeEC Advanced evaluation board apply equally to boards populated with a LatticeECP device. The same programming file can be used for either board.

The bitstream described in this document was developed using the Lattice FCRAM I Controller for the LatticeEC/ECP (FCRAM-ONE-E2-N1) and the LatticeXP (FCRAM-ONE-XM-N1) IP core. More information about this IP core can be found on the Lattice web site at www.latticesemi.com/ip.

Both the LatticeEC Advanced Evaluation Board and the LatticeXP Advanced Evaluation Board feature on-board FCRAM memory, TOSHIBA TC59LM806CFT-50.

See the user's manual of the respective board for further information about the FCRAM and other detailed specifications. The user's manuals can be downloaded from the Lattice web site at www.latticesemi.com/boards. Click on the appropriate board, then the user's manual link.

The following LatticeEC bitstream file is included in the evaluation package .ZIP file for the LatticeEC Advanced Evaluation Board:

- fcram_verilog_pnr_133MHz.bit

Two LatticeXP JEDEC files are included in the evaluation package .ZIP file for the LatticeXP Advanced evaluation board:

- fcram_verilog_pnr_133MHz.jed
- fcram_vhdl_pnr_133MHz.jed

Board Setup

For the LatticeEC Advanced Evaluation Board:

1. Set the V_{CCIO} pins of all banks to 2.5V by putting all eight jumpers of JP2-JP5 to JP4.
2. Push SW4 down.
3. Set all three pins (CFG2, CFG1, CFG0) of SW5 ON. (Push all SW5 pins down).
4. SW1 pin 1 is the rst_n reset signal. This must be pulled up to release the reset state.
5. For Rev-C PCB and later only: Located on the 3-pin header between SW4 and SW5. Select 2.5V by moving the jumper to the lower two pins.
6. The 33.33MHz oscillator must be installed in pins 2, 8 (GND), 9 (CLK) and 15 (3.3V) of the DIP-16 socket. This will provide a clock signal to the FPGA through ball F6.
7. Use a 5V power supply that can provide adequate current to the board.

For the LatticeXP Advanced Evaluation Board:

1. Set the V_{CCIO} pins of banks 0, 1, 6, 7 to 2.5V by moving all jumpers from JP1, JP2 or JP4 to JP3.
2. Install four jumpers on either JP7, JP9, or JP11 to select the correct core voltage for LFXP10C.
3. Set the pins (CFG1, CFG0) of SW4 OFF. (Pull the SW4 pins up).
4. SW1 pin 8 is the rst_n reset signal. This must be pulled up to release the reset state.
5. Enable the power circuit by installing a jumper between pins 2 and 3 of JP15-JP18:
Pins 2 and 3 of JP15 and JP16 are the left hand side two pins.
Pins 2 and 3 of JP17 and JP18 are the lower two pins.
6. The 33.33MHz oscillator must be installed in pins 1, 7 (GND), 10 (CLK) and 16 (3.3V) of the DIP-16 socket. This will provide a clock signal to the FPGA through ball A10.
7. Use a 5V power supply that can provide adequate current to the board.

Steps for Programming Bitstream Files into SPI Serial Flash

The following steps apply only to the LatticeEC Advanced Evaluation Board:

1. Connect your PC to the target board using a Lattice ispDOWNLOAD® Cable.
2. Launch ispVM® System software.
3. Click **File -> New**.
4. Click **Edit -> Add Device**.
5. Click **Select** and select **FPGA Loader** for “Device Family” and then click **OK**.
6. Highlight **Configuration Data Setup** and click the lower **Browse** to select either **fcram_verilog_pnr_133MHz.bit** or **fcram_verilog_pnr_166MHz.bit**.
7. Highlight **Flash Device** and click **Select...** to select **SPI Serial Flash, SPI-M25P80, 8-pin SOIC**, then click **OK**.
8. Click **OK** again to close the FPGA Loader window.
9. Make sure the SW4 switch is in the UP position and the ispDOWNLOAD cable is connected to either JP6 or JP8.
10. Click **GO** to program bit to SPI flash.
11. Push SW4 back to DOWN position.

For the LatticeXP Advanced Evaluation Board, ispVM System can be used to directly program the LatticeXP device with a Lattice ispDOWNLOAD Cable.

Memory Testing Algorithm

This test is completed by writing test_data into the address space of the user interface (from 0 to 1FFFFFFE), then reading the data back to check for errors.

The test starts by writing 0x01 to byte_1 (D15-D8) and 0xfe to byte_0 (D7-D0) of address 0x0000000. The test data is then rotated within the byte and the address is increased by two for the next write cycle.

When the write reaches address 0x1fffffe, reading and verification will begin, starting at address 0x0000000, then address 0x0000002, etc. (see below).

After the read reaches address 0x1ffffe, one test cycle is considered complete. The test_data will then be changed for the next test.

In order to prevent writing the same pattern to the same address location for every test, the test_data is rotated and then inverted at address 0x000000 before a new test starts.

The testing sequence is as follows:

	byte_1 D15-D8	byte_0 D7-D0
Test 1 start-----		
Write to address 0x000000:	0x01	0xfe
Write to address 0x000002:	0x02	0xfd
Write to address 0x000004:	0x04	0xfb
Write to address 0x000006:	0x08	0xf7
Write to address 0x000008:	0x10	0xef
Write to address 0x00000a:	0x20	0xdf
Write to address 0x00000c:	0x40	0xbf
Write to address 0x00000e:	0x80	0x7f
Write to address 0x000010:	0x01	0xfe
Write to address 0x000012:	0x02	0xfd
Write to address 0x000014:	0x04	0xfb
Write to address 0x000016:	0x08	0xf7
:		
:		
Write to address 0x1ffffe:	0x80	0x7f
Read from address 0x000000		
Read from address 0x000002		
:		
:		
Read from address 0x1ffffe		
Test 2 start-----		
Write to address 0x000000:	0xfd	0x02
Write to address 0x000002:	0xfb	0x04
Write to address 0x000004:	0xf7	0x08
Write to address 0x000006:	0xef	0x10
Write to address 0x000008:	0xdf	0x20
Write to address 0x00000a:	0xbf	0x40
Write to address 0x00000c:	0x7f	0x80
Write to address 0x00000e:	0xfe	0x01
Write to address 0x000010:	0xfd	0x02
Write to address 0x000012:	0xfb	0x04
Write to address 0x000014:	0xf7	0x08
Write to address 0x000016:	0xef	0x10
:		
:		
Write to address 0x1ffffe:	0xfe	0x01
Read from address 0x000000		
Read from address 0x000002		
:		
:		

Read from address 0x1ffffffe

Test 3 start-----

Write to address 0x00000:	0x04	0xfb
Write to address 0x00002:	0x08	0xf7
Write to address 0x00004:	0x10	0xef
Write to address 0x00006:	0x20	0xdf
Write to address 0x00008:	0x40	0xbf
Write to address 0x0000a:	0x80	0x7f
Write to address 0x0000c:	0x01	0xfe
Write to address 0x0000e:	0x02	0xfd
Write to address 0x00010:	0x04	0xfb
Write to address 0x00012:	0x08	0xf7
Write to address 0x00014:	0x10	0xef
Write to address 0x00016:	0x20	0xdf

:

:

Write to address 0x1ffffffe:	0x02	0xfd
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Read from address 0x0000000

Read from address 0x0000002

:

:

Read from address 0x1ffffffe

Test 4 start-----

Write to address 0x0000000:	0xf7	0x08
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:

:

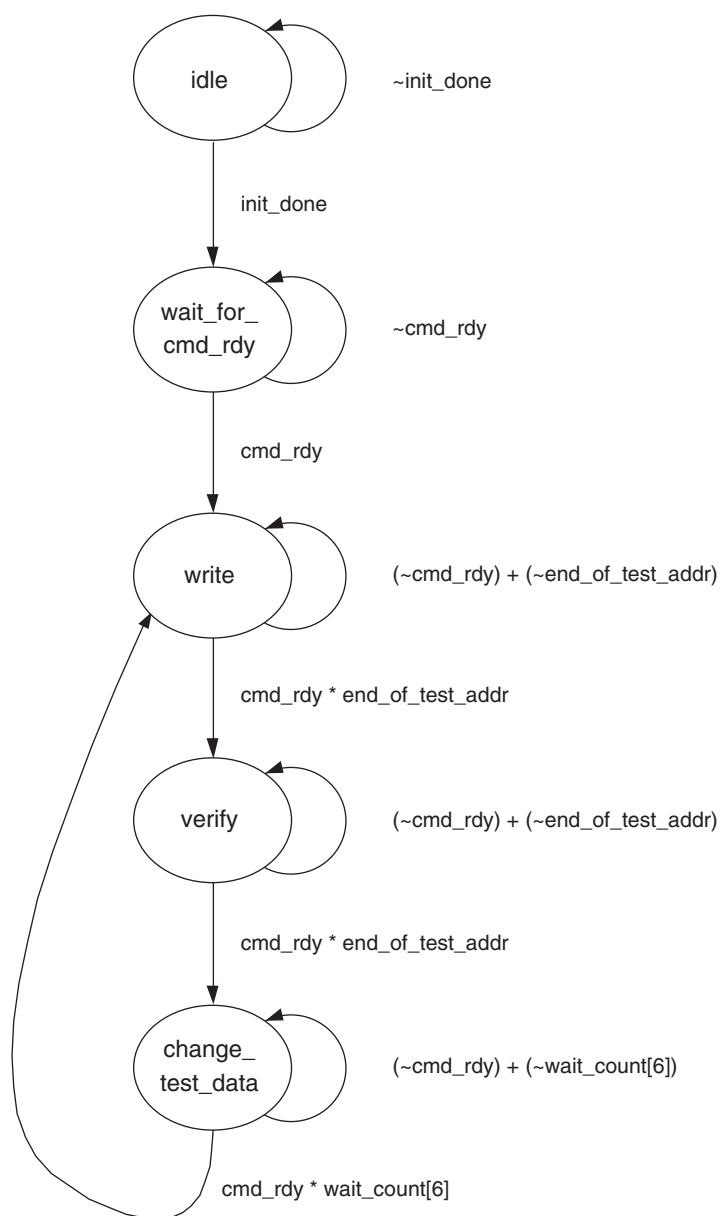
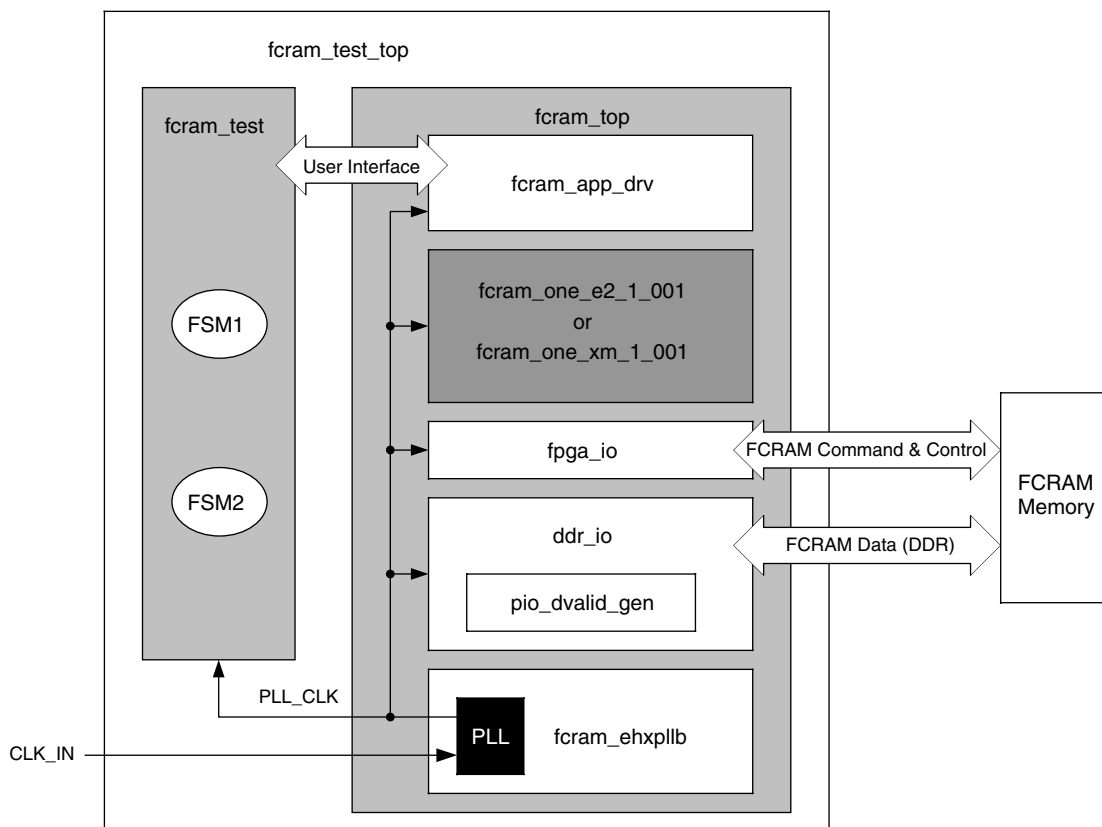
Figure 1. FSM1 State Machine Diagram of the FCRAM Test Cycle

Figure 2. Block Diagram of the FCRAM Test Program

Test Results

Two counters are implemented to show the number of successful and/or failed tests. The failure counter is increased by one when data in any address location is incorrect. The success counter is increased only if all the data in all address locations are correct.

- `number_of_tests_passed` is displayed on LEDs D8, D7, D6, D5
- `number_of_tests_failed` is displayed on LEDs D4, D3, D2, D1

Waveform Measuring

For measuring write cycle or read cycle timing, set a trigger at the rising edge of signal `fsm2`. This signal is assigned to ball AE10 (signal `fsm2`) for the LatticeEC Advanced Evaluation Board and ball F3 for the LatticeXP Advanced Evaluation Board. After the rising edge of `fsm2`, the FCRAM cycle will be changed from a write cycle to a read cycle. The following images are FCRAM waveforms captured on a LatticeEC Advanced Evaluation Board using a Tektronix digital scope. The upper waveform is the `fsm2` signal and the lower waveform is the DQS signals.

Tek PreVu

Δ: 20.0mV
@: 2.74 V
Δ: 113ns
@: 172ns

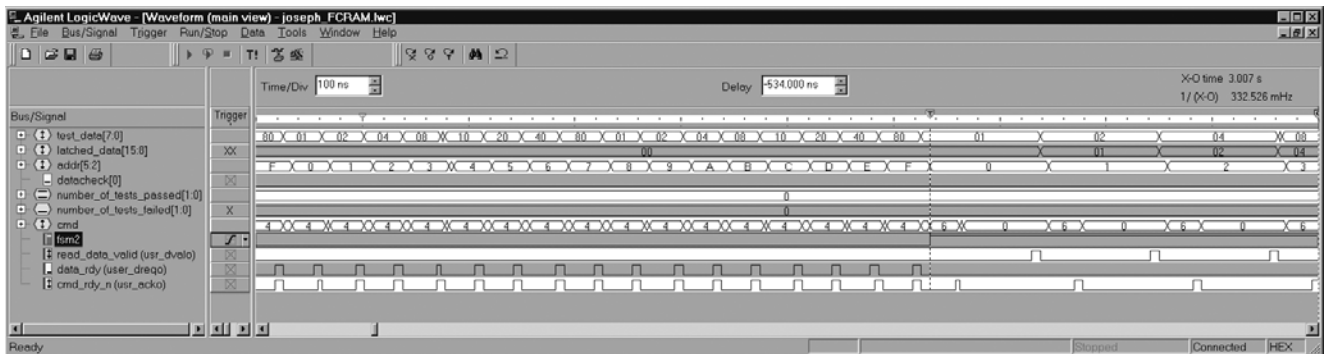
Ch1 Freq 133.6MHz

Ch1 1.00 V Ω Ch2 2.00 V M 40.0ns A Ch2 960mV

29 Jun 2005 12:53:33

18.20 %

Figure 4. User Side Write to Read Timing



Agilent LogicWave - [Waveform (main view) - joseph_FCFRAM.tvc]

File Bus/Signal Trigger Run/Stop Data Tools Window Help

Time/Div 100 ns Delay -534.000 ns X0 time 3.007 s 1/(x-0) 332.526 mhz

Bus/Signal

- test_data[7:0]
- latched_data[15:0]
- add[5:2]
- datacheck[0]
- number_of_tests_passed[1:0]
- number_of_tests_failed[1:0]
- cmd
- read_data_valid (usr_dvld)
- data_rdy (user_dreq)
- cmd_rdy_n (usr_ack)

Trigger

10 20 40 60 80 FD X FB X F7 XEF

08 10 20 40 60 80

C X D X E X F X

0 1 2 3

0 1

0 5 0 5 0 5 0 5

4 4 4 4 4

Ready Stopped Connected HEX

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com